REMARKS

By this Amendment, Claims 20-50 are pending, with Claim 20 as the only independent claim. Applicant believes all pending claims are now in condition for allowance which is respectfully requested.

1. Objection to Specification

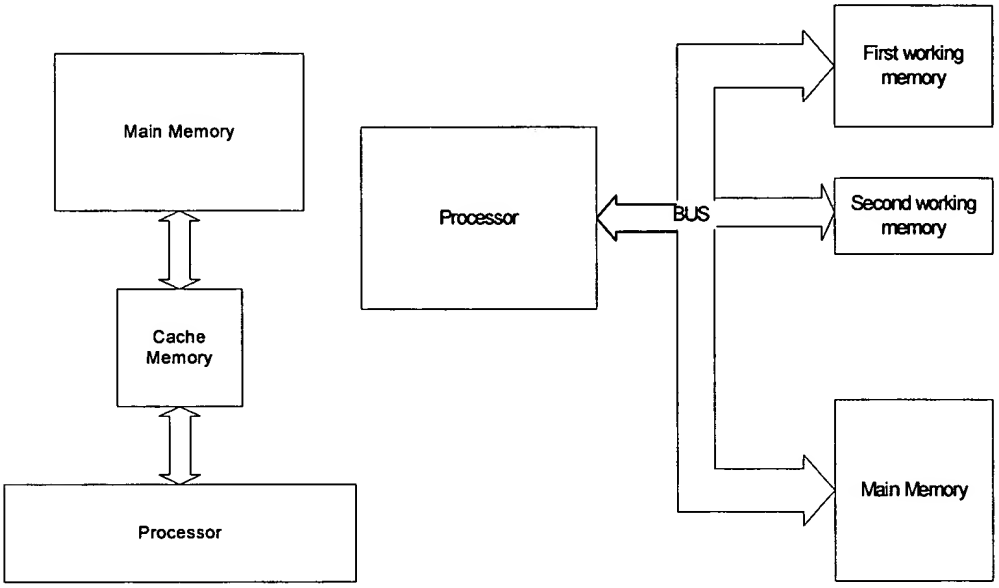
Applicant has amended the title of the application to be more descriptive. Reconsideration and withdrawal of this objection is respectfully requested.

2. Rejections under 35 U.S.C. § 103

The Examiner rejects claims 20, 21, 23, 24, 27-36, 40, 41 and 50 as being unpatentable over Okin, U.S. Patent No. 5,361,337 (hereinafter referred to as "Okin") in view of Fletcher et al., U.S. Patent No. 5,012,409 (hereinafter referred to as "Fletcher"). Without acceding to the Examiner's rejection, Applicant has amended the claims in hopes of receiving a quick allowance of the pending claims. Applicant reserves the right to pursue additional claims in a continuation or divisional application.

Claim 1 has been amended to require that the processor in the unpredictable microprocessor or microcomputer processes instructions from the main memory, first working memory or second working memory. The main memory includes an operating system, a main program and a secondary program, wherein the main program is not related to the secondary program. In addition, claim 1 recites that a bus connects the processor to the main memory, the first working memory and the second working memory. The switching means make the processor unpredictable by switching from one of the two working memories to the other working memory at a random interrupt. As the processor is unpredictable, security of the microprocessor is enhanced.

In Okin, the cache memory is placed between the processor and the main memory (Okin, Col. 1, lines 19-21, Col. 2, lines 8-20). This architecture is reproduced below.



Okin Present Invention

The Okin architecture is completely different from the architecture described and claimed in the present application, as shown by Fig. 1 of the present application simplified in the drawing above. According to the amended claim 20 of the present invention, the processor, main memory and the working memories are *connected by a bus*. Neither Okin nor Fletcher disclose a bus connecting a processor, main memory, first working memory and second working memory.

According to Okin, during execution of the software program, the cache memory stores the most frequently utilized instructions and data. Whenever the processor needs to access information memory, *the processor examines the cache first before accessing the main computer memory*. The second process in Okin is executed

only when a cache miss occurs. Since the cache memory is not the main memory, then the cache memory in Okin must be likened to a working memory. Registers absolutely cannot be likened to a working memory. Therefore, there is only one working memory in Okin, the cache. The claims of the present invention require a *second working memory*, which is not taught or suggested by the disclosure in Okin.

Furthermore, Okin does not suggest switching means for switching, *at a random interrupt*, while the programs are running, from one of the two working memories to the other working memory. Okin discloses no means of generating a random interrupt, much less switching upon the occurrence of a random interrupt.

Okin discloses a processor switching between processes, and not a processor switching between memories as is taught by the Applicant. In Okin, the two different processes, each being the result of a program, can be executed in the same memory. Accordingly, switching between processes is different than a processor switching between two working memories as required by the claims of the present invention. Okin does not teach or suggest a bus for connecting the processor to the main memory and to the two working memories, since Okin is only directed to switching between processes.

In addition, Okin does not teach or suggest at least one block of registers for storing the operating context of the programs in the main memory. Registers taught by Okin are *inside* the processor, and do not store the context of the programs in the main memory.

Finally, amended claim 20 requires that the main program and the secondary program are not related. This is taught in the present specification at Page 12, lines 18-19, stating "interruption, (31) causing changeover from normal operation under control of program (P1) to operation in the dummy mode under the control of program (P2)."

Main program P1 and secondary program P2 are further discussed at Page 14, lines 8-19, stating "when main program (P10 needs to be protected, by its own diversion of a secondary program (P2), it trips and generates a random length... The operation of the process can then be controlled by the secondary program (P2) which , for example, can trigger a waiting loop of which the length of time depends on a random number derived from the generator (2)." Page 15, lines 4-5 state "the secondary program does not execute any function mandatorily related to the main program." None of the cited references teach this feature.

Even if the features of the dependent claims are considered not new or obvious by the Examiner, at least by virtue of their dependency from Claim 20, the combination of features claimed is new and non-obvious.

The Examiner rejects Claims 22, 25, 26, 37, 39, 42-49 as being unpatentable over Okin in view of Fletcher, and further in view of Griffin III et al. U.S. Patent No. 5,249,294 (hereinafter referred to as "Griffin"). Applicant respectfully traverses said rejection.

The Griffin disclosure is directed to preventing compromise of a secure data processing routine by a procedure known as a "clock attack" (Griffen col. 1, l. 12-14). Griffen discloses the step of randomly varying the duration between occurrence of an externally observable event and the execution of a predetermined routine. This purpose is disconnected from the purpose of Okin, which is directed to processing efficiency. This purpose is also disconnected from the purpose of Fletcher, which is directed to an operating system for a multi-tasking operating environment. The Examiner asserts that one skilled in the art would have incorporated the operating system of Fletcher with Okin to coordinate processes, in addition to incorporating the security features of Griffin. However, the system in Okin is intended to increase

processing efficiency, while the random interrupts that cause the processor in the present invention to be unpredictable actually slow down processing. One skilled in the art would not have been motivated to combine the cited references to create a slower processor.

Griffin does not teach or suggest any means *connected to a* bus for de-correlating the running of a main program and secondary program from an isochronous clock, wherein the bus connects the processor to the main memory and to the two working memories that are used by the processor for executing instructions.

Inasmuch as the combination of Okin and Fletcher do not teach or suggest the present invention, Applicant respectfully submits Claim 20 and all claims dependent thereon are neither anticipated nor rendered obvious in view of Okin and Fletcher.

Applicant respectfully requests reconsideration of the application and withdrawal of the rejection of all pending claims in view of the foregoing arguments. All pending claims are believed to be in condition for allowance and passage of the application to issue at an early date is earnestly solicited.

The Commissioner is hereby authorized to charge to deposit account number 50-1165 and fees not included herein, under 37 CFR §§ 1.16 and 1.17, that may be required by this paper and to credit any overpayment to that Account. A duplicate copy of this page is included for such purpose. If any additional extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

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Date

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